

REMARKS

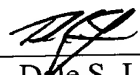
The specification is amended to change references of "Fig. 1" to -- Figs. 1A and 1B -- to properly reflect the changes made to the drawings in the formal drawings filed on July 27, 2001, and to delete reference to a non-existent "Fig. 4".

Applicants believe that the claims are in condition for allowance and request that the application be processed to issue. If any questions remain, the Examiner is respectfully invited to contact the undersigned.

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached Appendix is captioned "Version with markings to show changes made."

Respectfully submitted,

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Enclosure: Appendix

*a*

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

On page 4, lines 18-27, the paragraph beginning “As shown in **Fig. 1**, an embodiment of the route switch ...” was amended as follows:

(Amended) As shown in [**Fig. 1**] **Figs. 1A and 1B**, an embodiment of the route switch packet architecture according to one aspect of the invention comprises Bi-directional Access Port (BAP) **10**, Host Packet Injection (HPI) **14**, Flexible Data Input Buffer (FDIB) **20**, Test **28**, Clock & PLLS **30**, Analysis Machines (AMs) **42,56,70,84**, Packet Task Manager (PTM) **98**, Global Access Buses (GAB) **108,110,112,114,116,118**, External Memory Engines (EME) **120,156**, Internal Memory Engines (IME) **122,152**, Packet Manipulator (PM) **126**, Hash Engine (HE) **158**, Centralized Look-Up Engine Interface (CIF) **160**, Flexible Data Output Buffer (FDOB) **162**, and Search/Results/Private **166,168**. With the exception of Search/Results/Private **166,168**, the combination of the above described elements may be considered a multi-thread packet processor.

On page 36, lines 14-18, the paragraph beginning “**Fig. 4** shows a block diagram that depicts one implementaion ...” was amended as follows:

(Amended) [**Fig. 4** shows a block diagram that depicts one implementaion of the architecture of the EME.] There are two asynchronous boundaries. The first is in the GAB controller, which synchronizes between the internal multi-thread packet processor clock (RSP2CLK) and the local clock (MEMCLK) to run the EME core. The second is in the high-speed access port (HSAP) controller for PM **126**.

End of Appendix

*a*